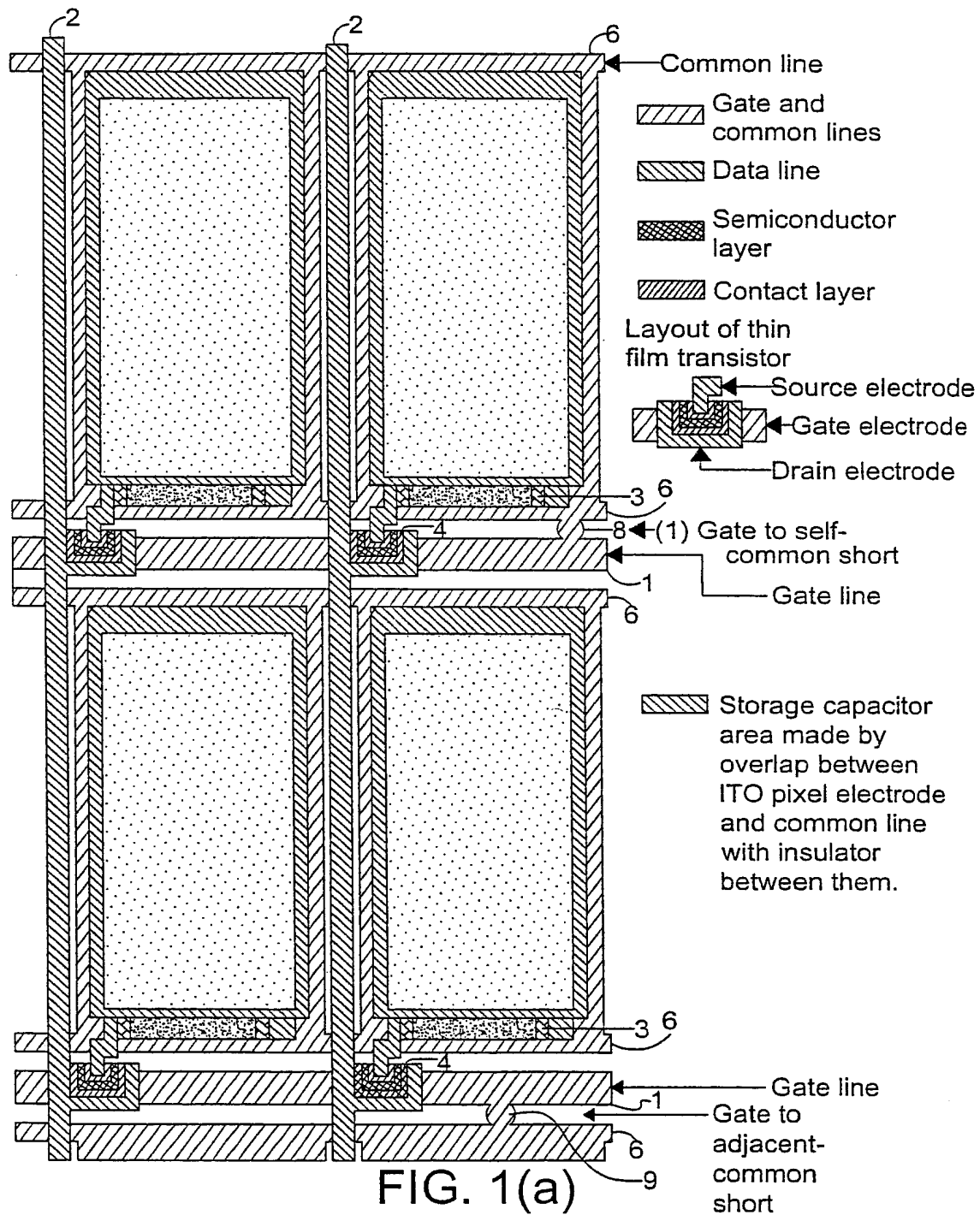


Gate to common short defects in TFT array with double common line layout.



Explanation of pixel layout by showing four pixels in different process step.

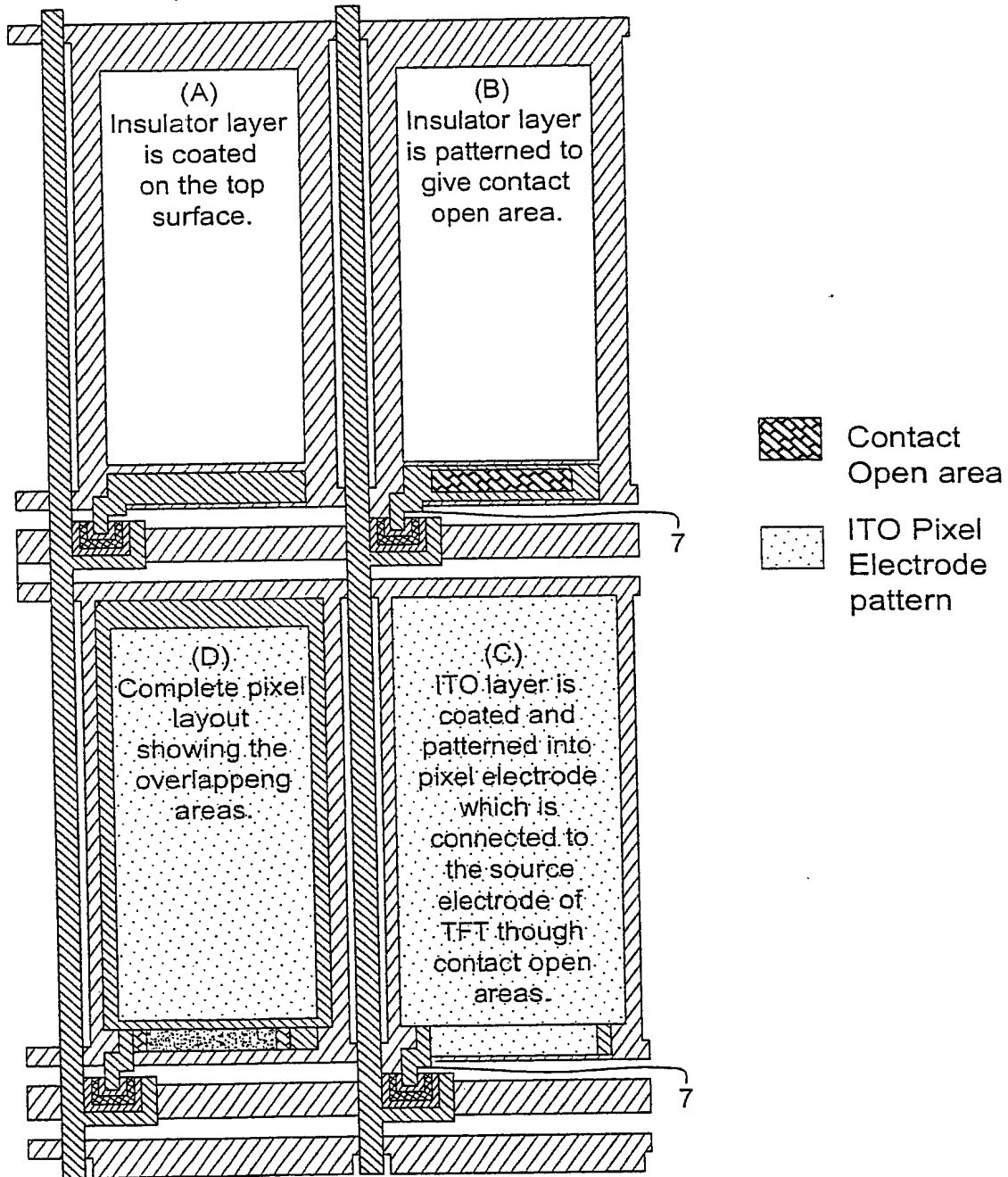


FIG. 1(b)

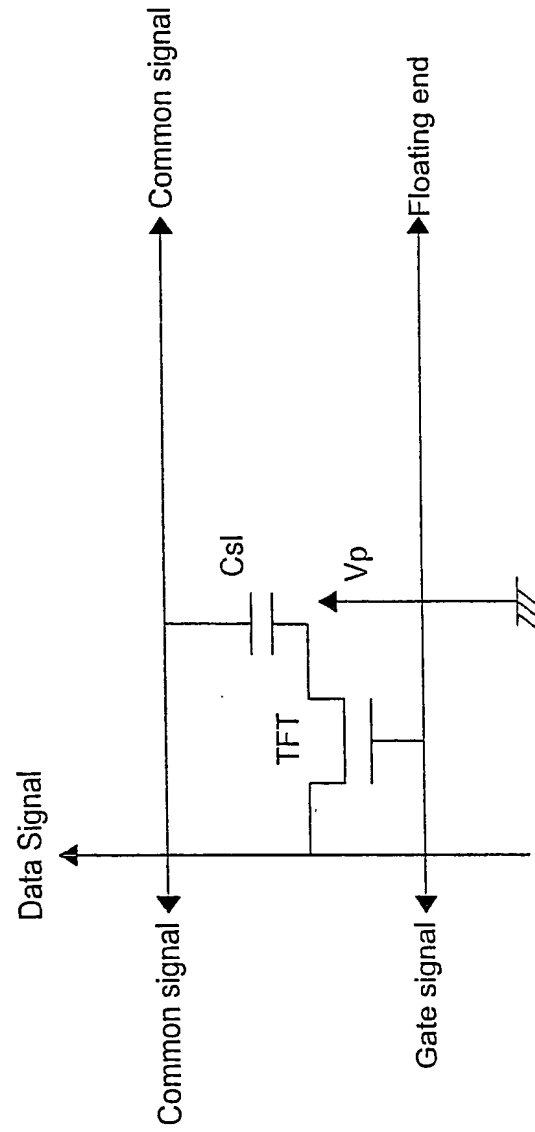


FIG. 2

Simplified equivalent circuit of one cross point in TFT array

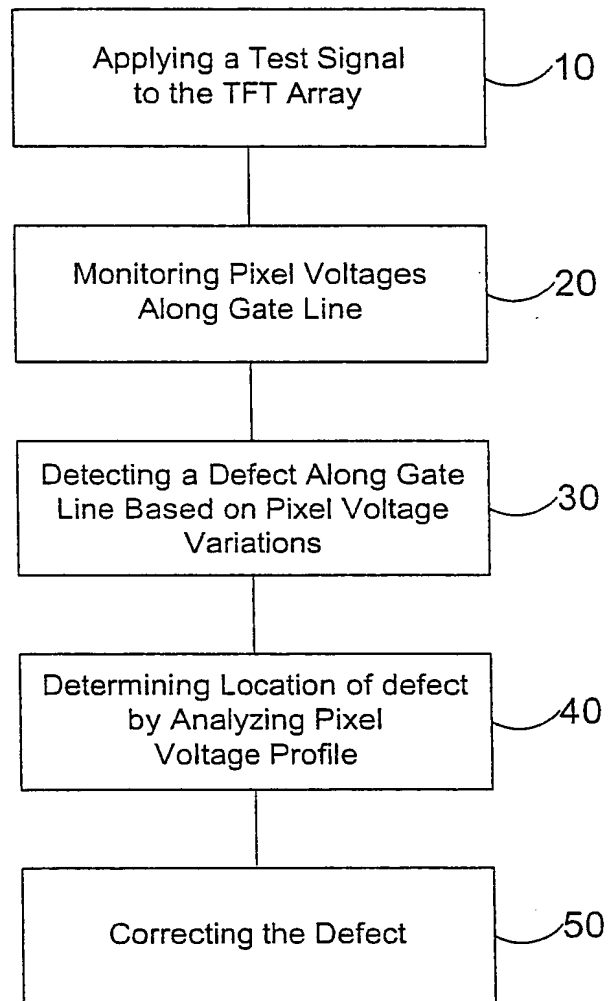


FIG. 3

Signal patterns to detect the short defect between gate and common lines.

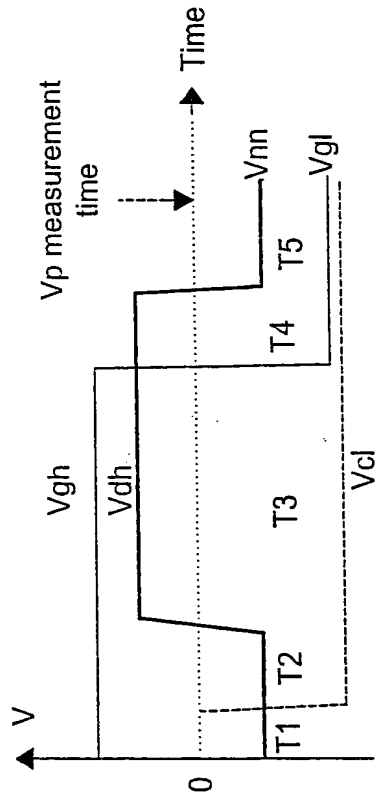


FIG. 4(a)

Signal patterns for positive pixel voltage

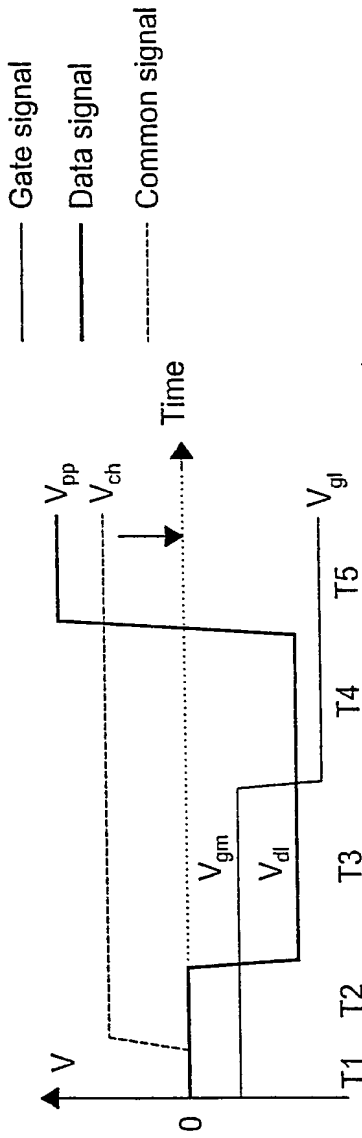


FIG. 4(b)

Signal patterns for negative pixel voltage

Analysis of pixel voltages along the gate line with a short defect between gate and self-common lines when the signal patterns of Fig. 4 (a) is applied.

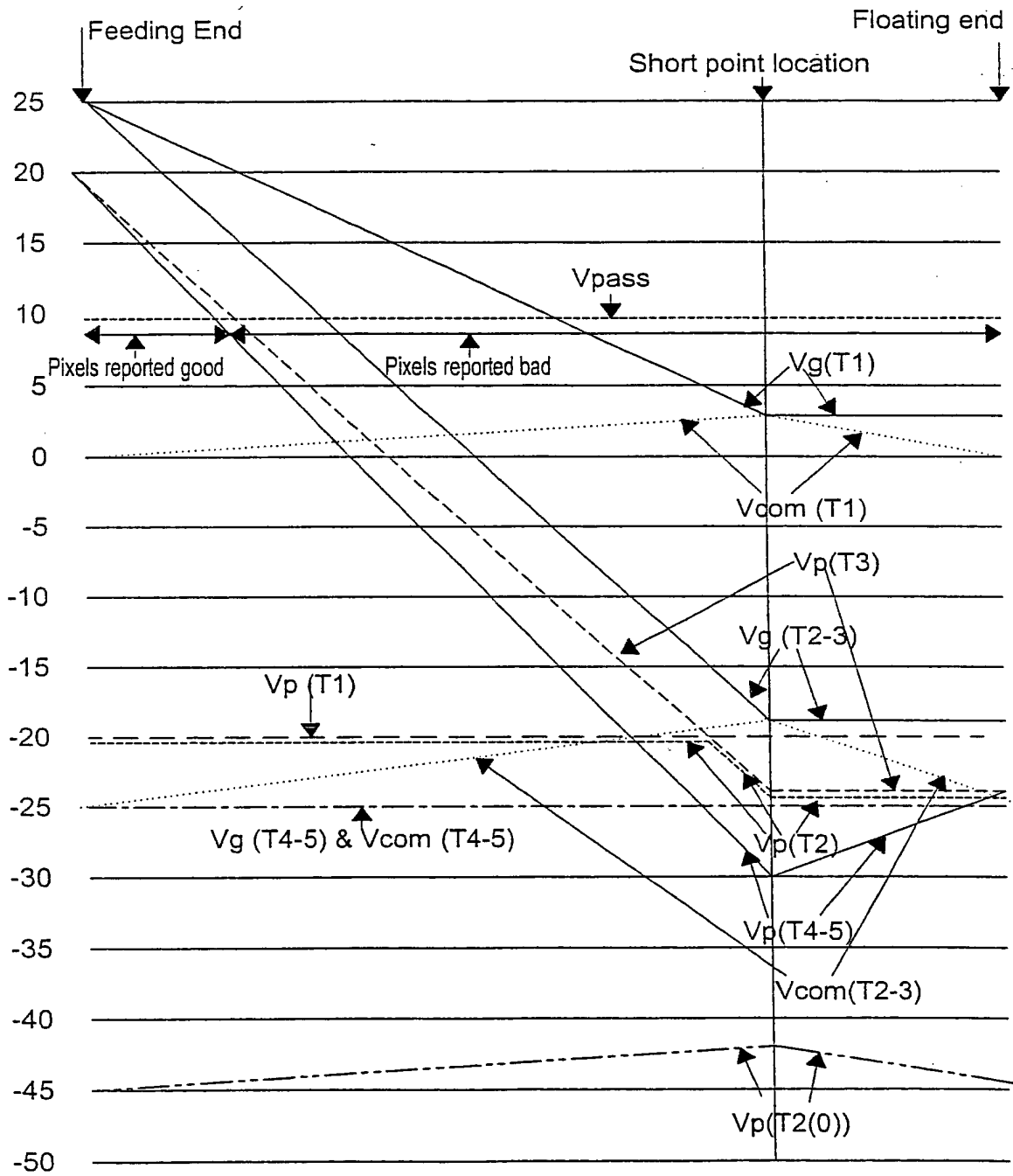


FIG. 5

Analysis of pixel voltages along the gate line with a short defect between gate and self-common lines when the signal patterns of FIG. 4 (b) is applied.

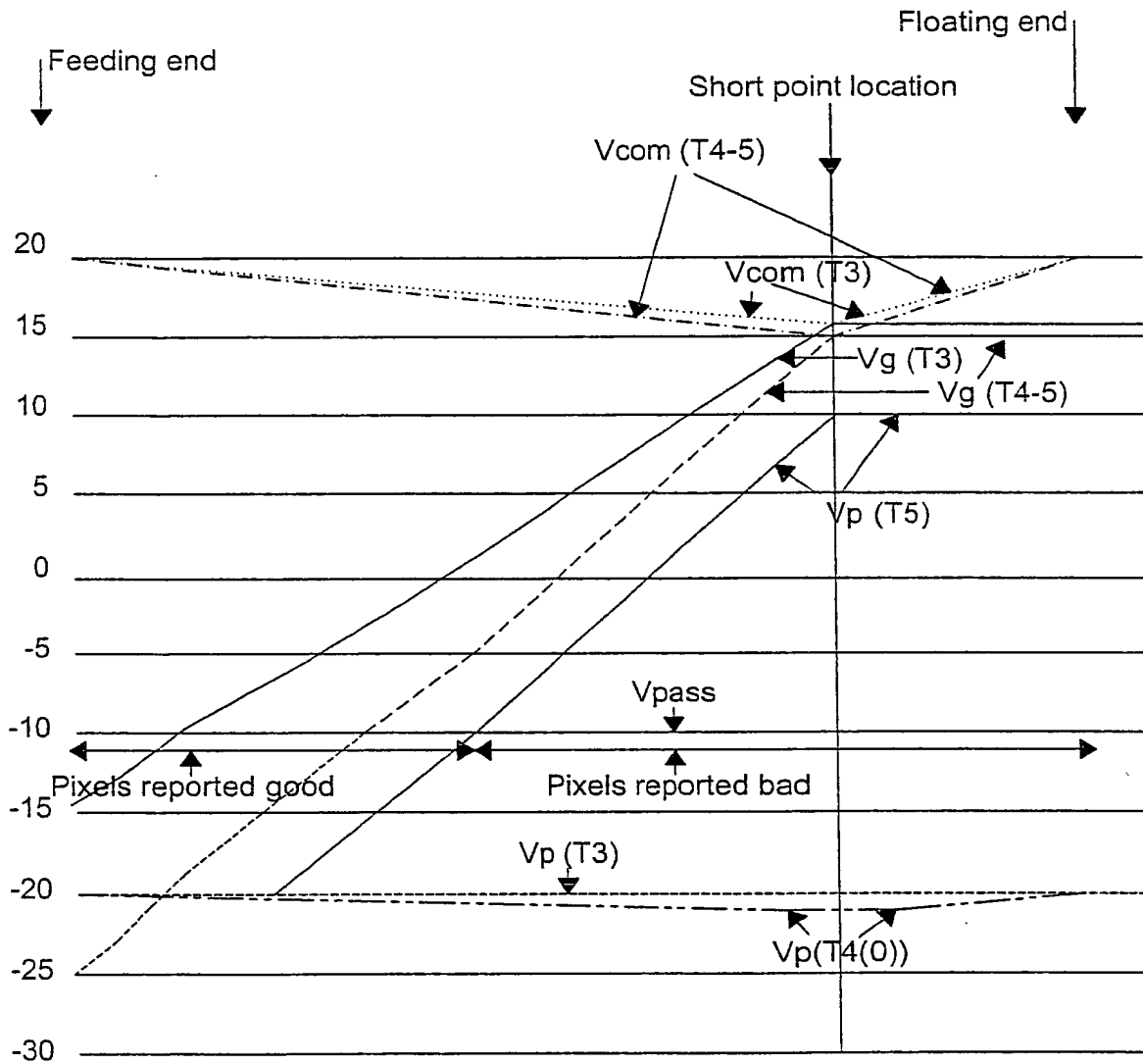


FIG. 6

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Calculation of pixel voltages (V_p (T4-5) of Fig. 5 - V_p (T5) of Fig. 6) along the gate line with a short defect between gate and self-common lines.

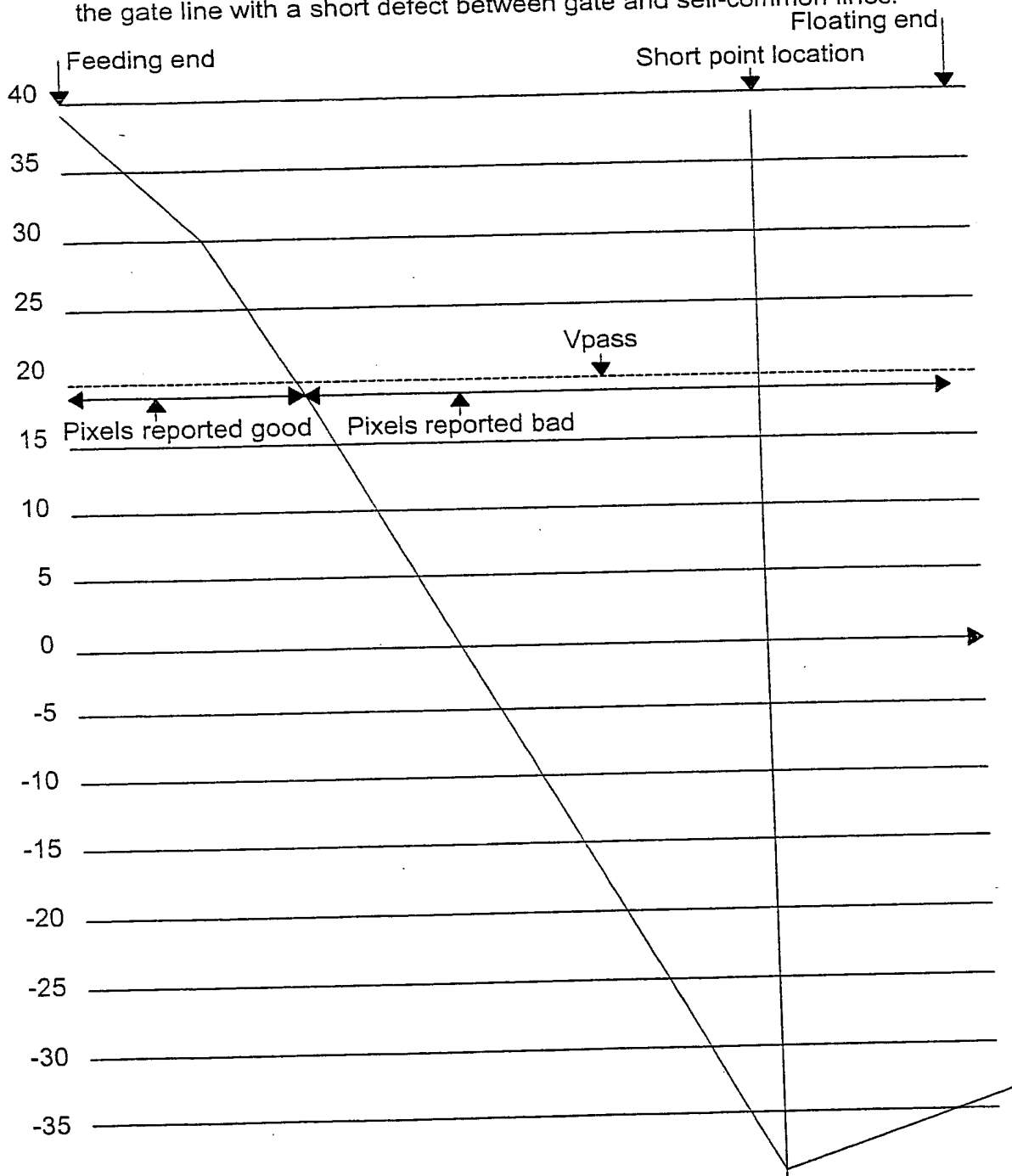


FIG. 7

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Analysis of pixel voltages along the gate line with a short defect between gate and adjacent-common lines when the signal patterns of Fig. 4 (a) is applied.

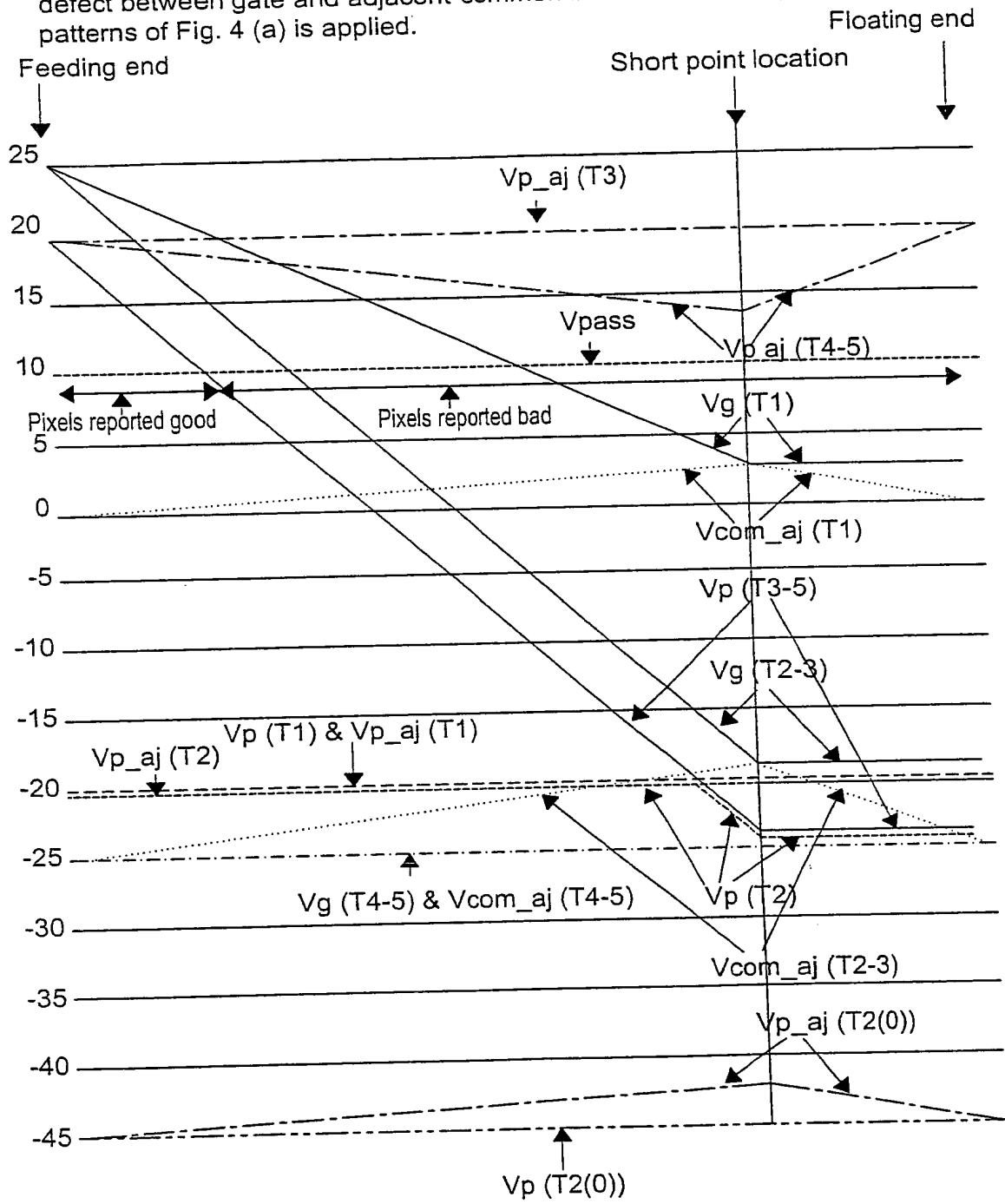


FIG. 8

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Analysis of pixel voltages along the gate line with a short defect between gate and adjacent-common lines when the signal patterns of FIG. 4 (b) is applied.

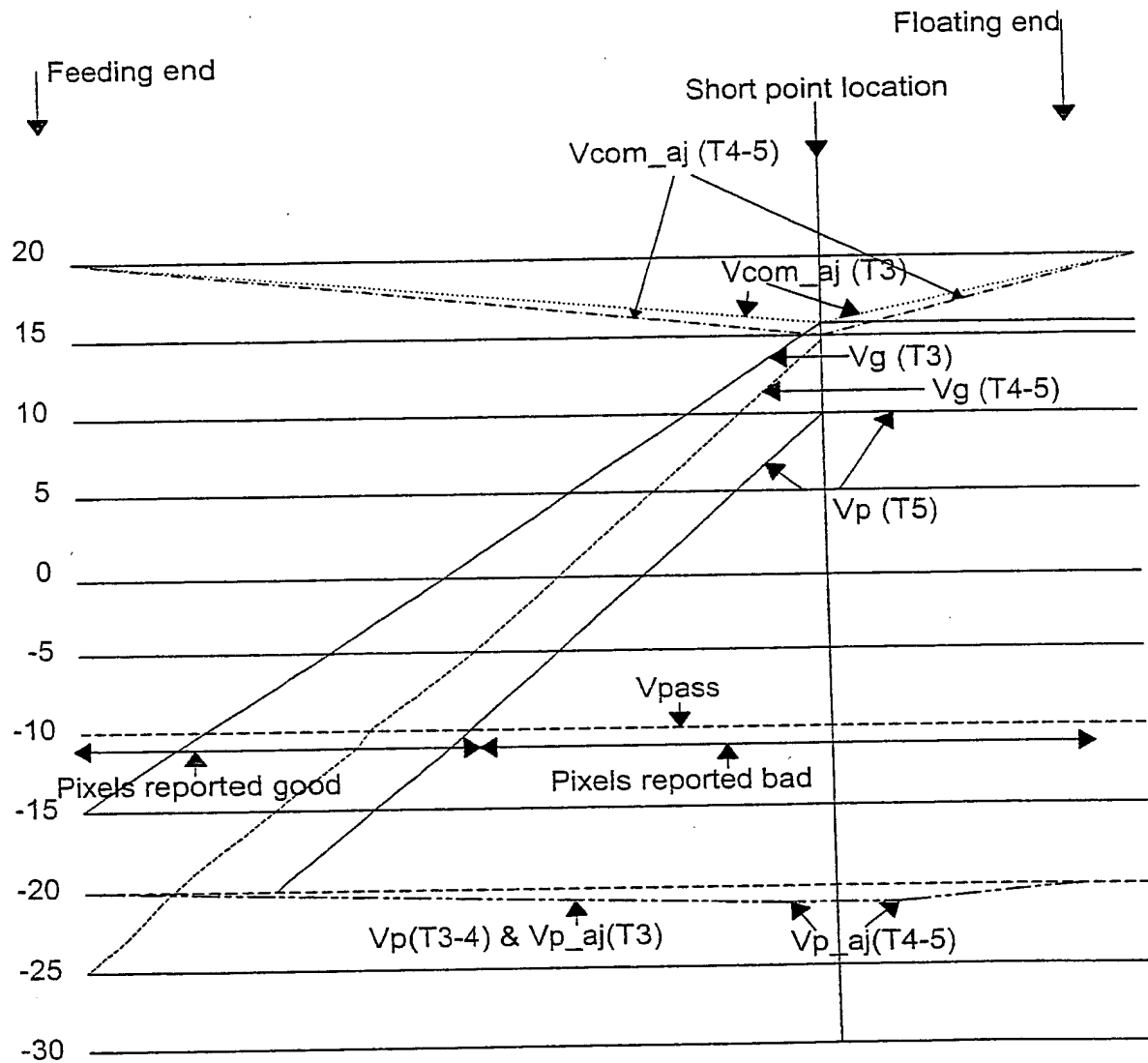


FIG. 9

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Calculation of pixel voltages (V_p (T3-5) of Fig 8- V_p (T5) of Fig 9) along the gate line with a short defect between gate and adjacent-common lines.

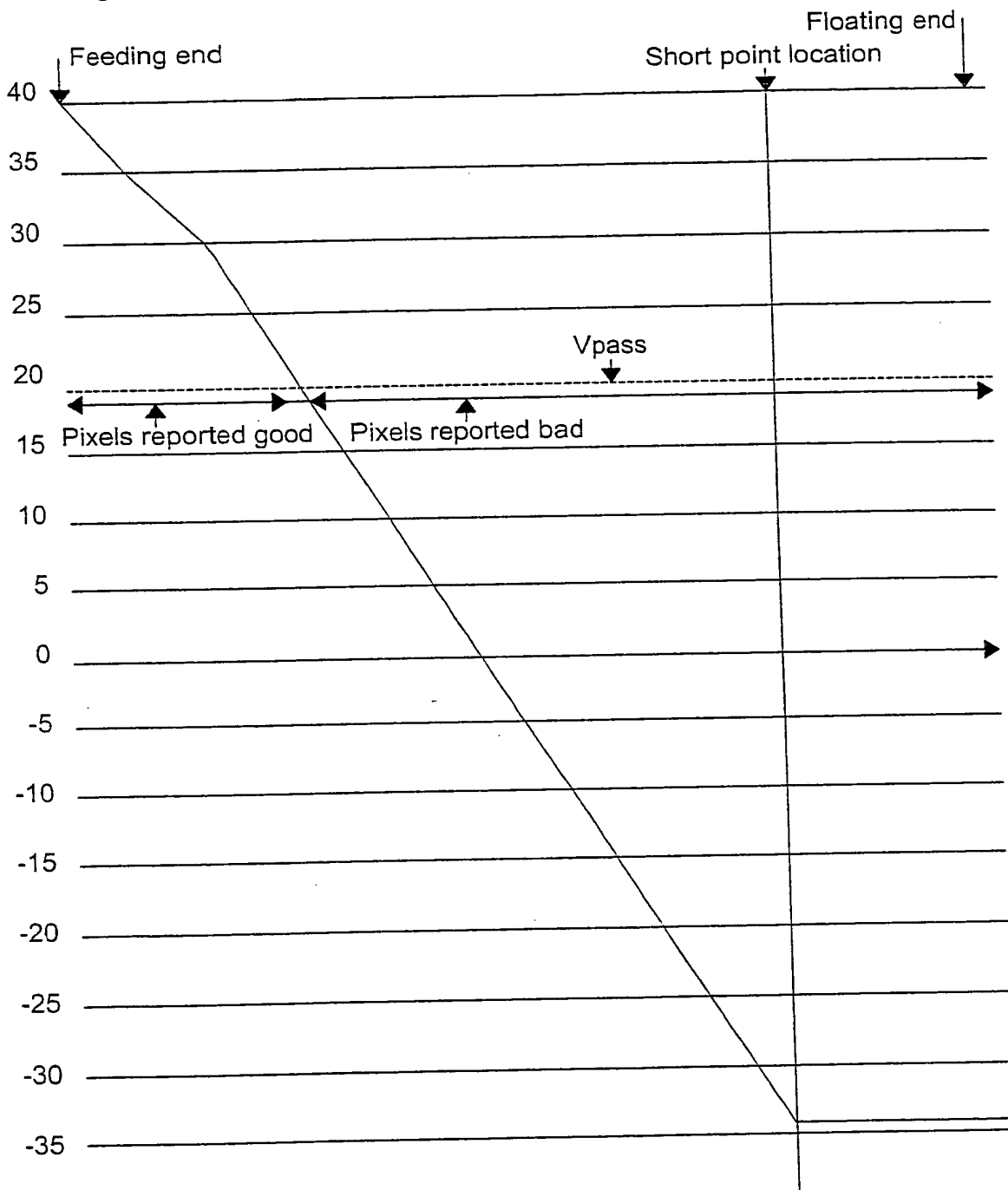


FIG. 10

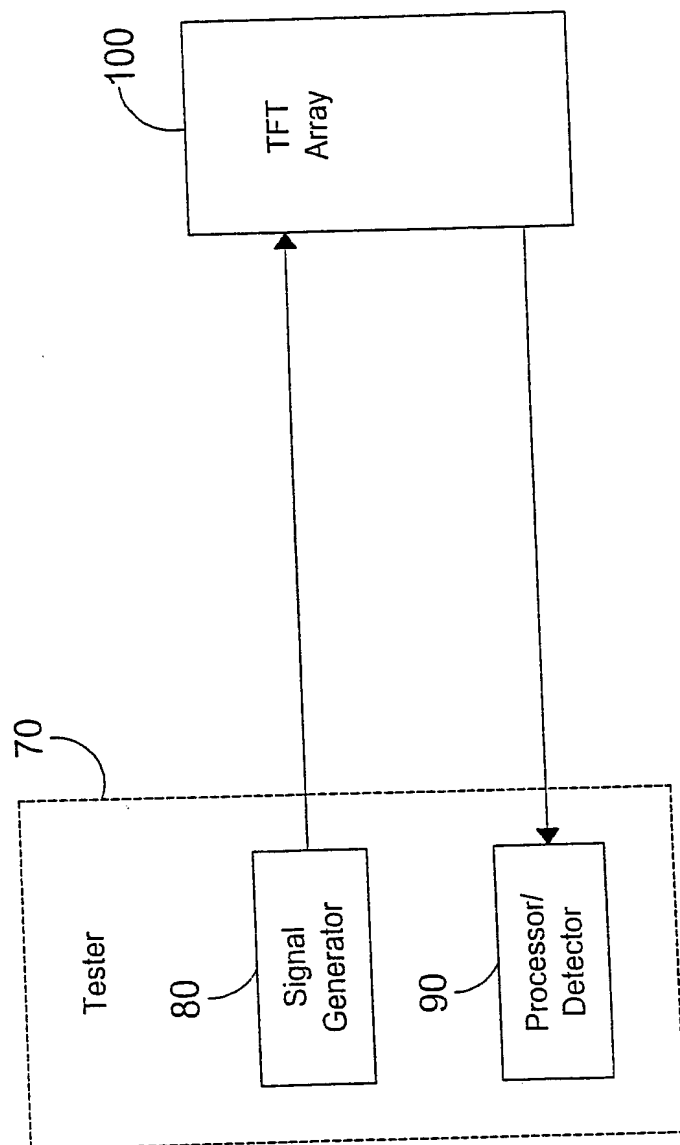


FIG. 11

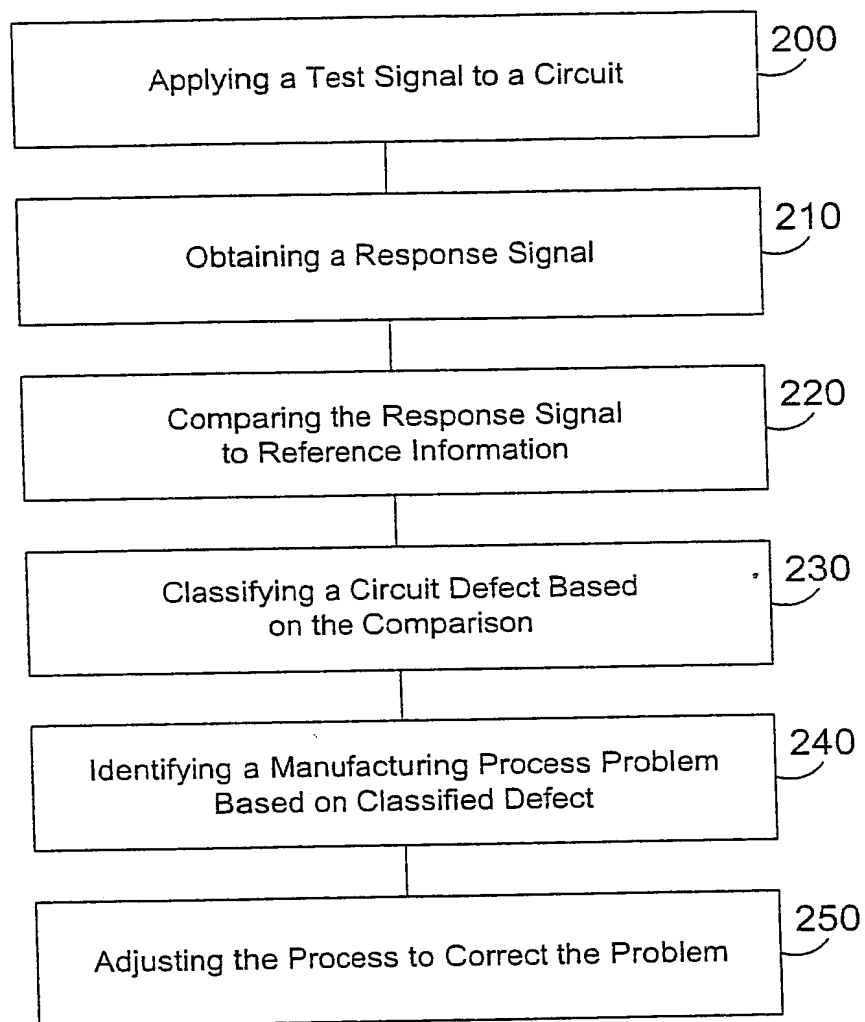
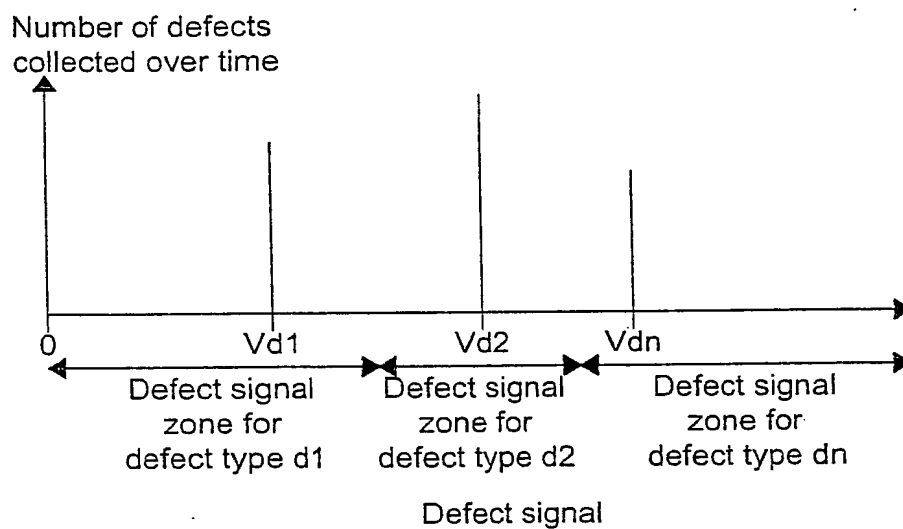


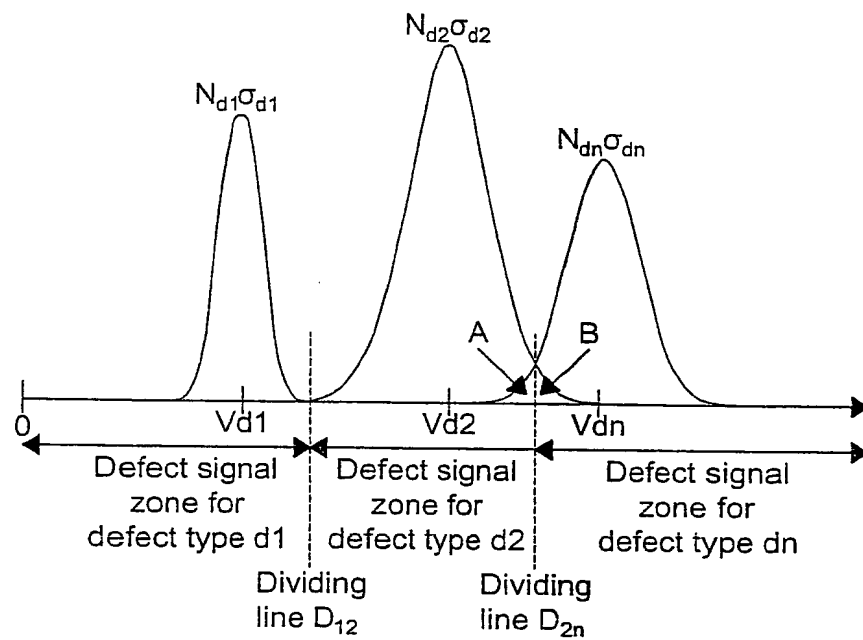
FIG. 12

Defect Histogram that was obtained using ideal distribution of defect signals for defects d_1 , d_2 , and d_n , where V_{d1} , V_{d2} , and V_{dn} are the representative defect signals for d_1 , d_2 and d_n , respectively, and the defect signal zones for the defects d_1 , d_2 and d_n .



Defect signal
FIG. 13

Realistic distribution of the defect signals for the defects d_1 , d_2 and d_n , where normal distribution function is used for each defect type.



Defect signal
FIG. 14

Explanation of pixel layout by showing four pixels in different process step.

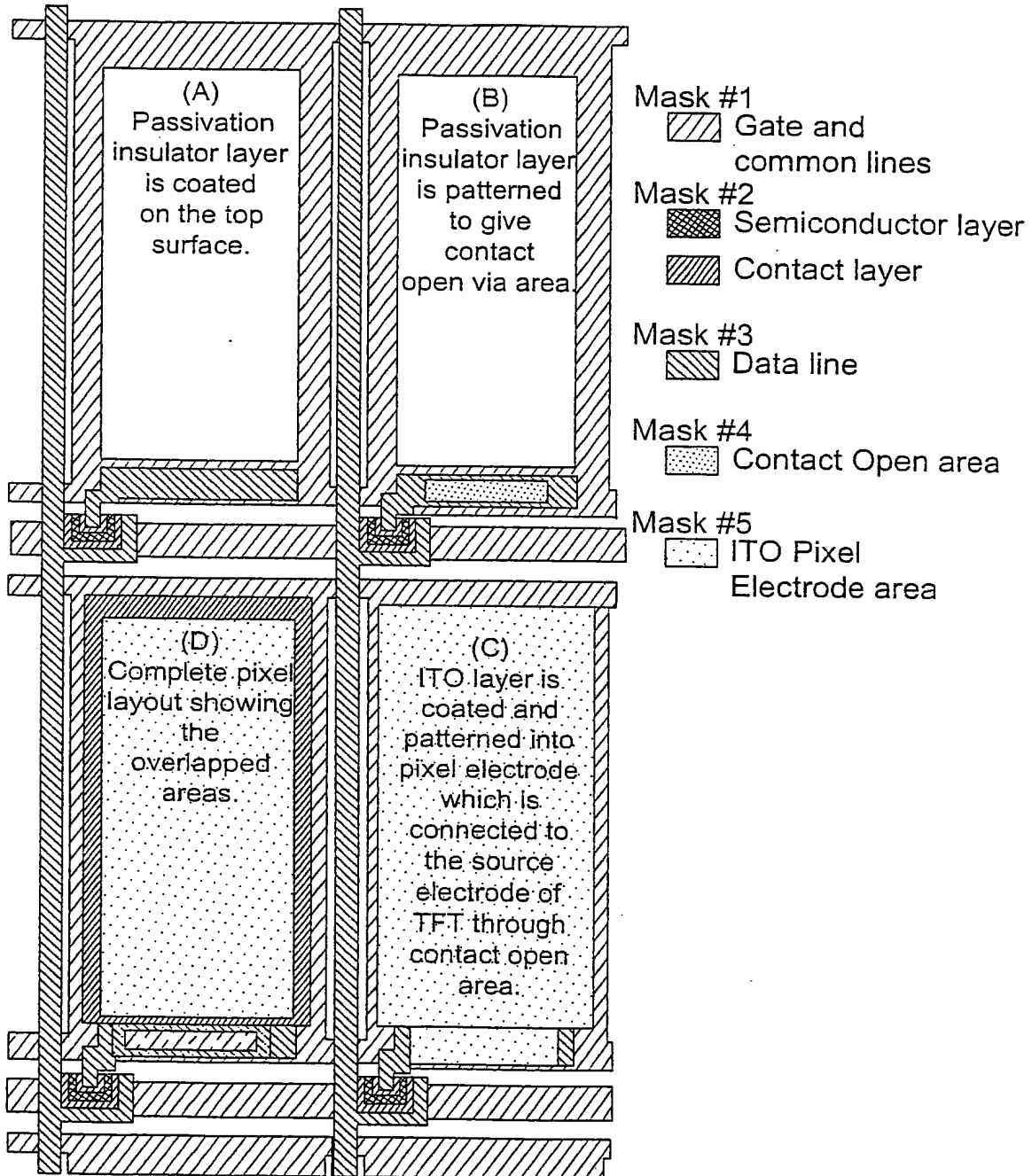


FIG. 15

Example of the process flow for TFT-array

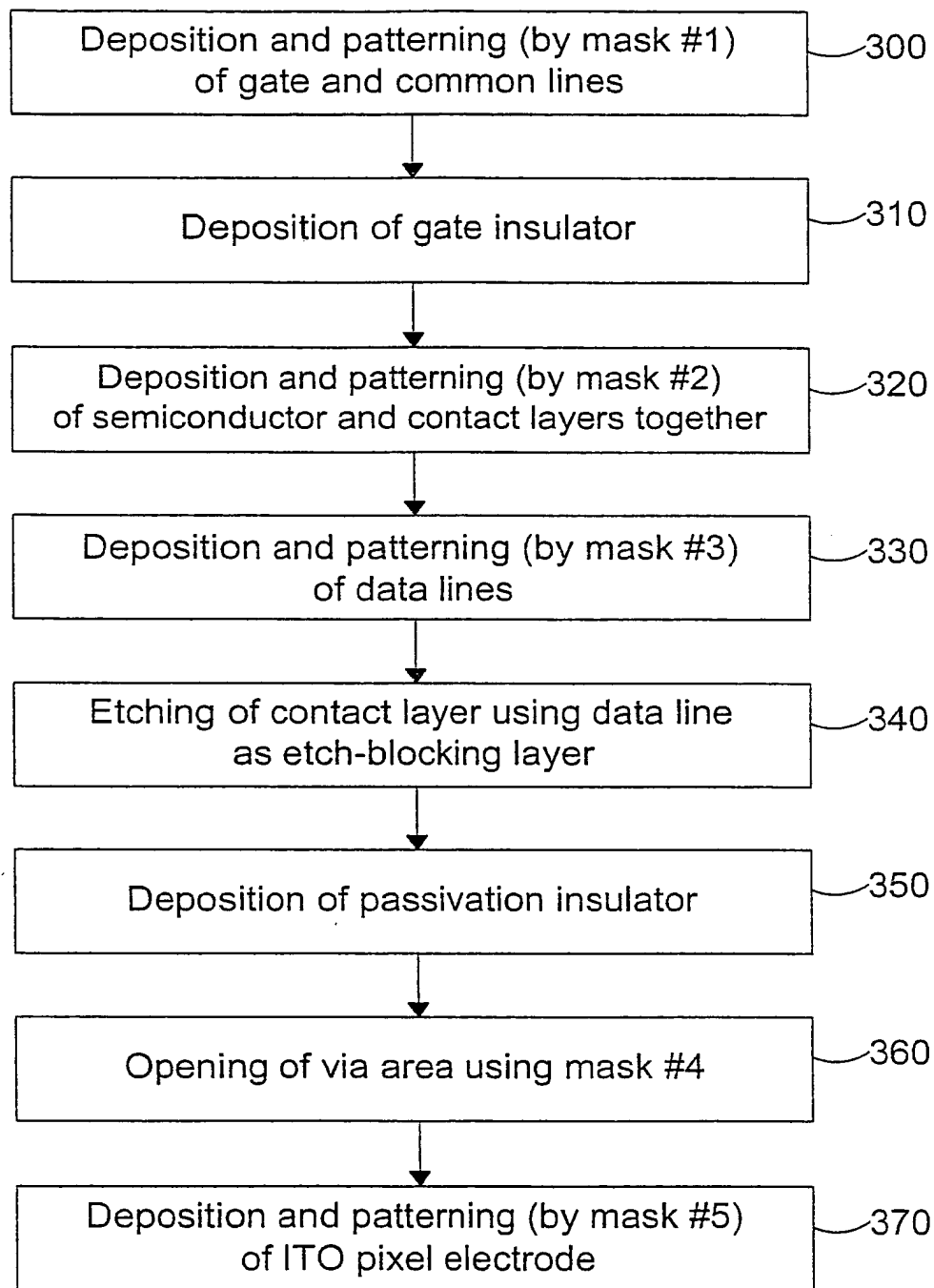


FIG. 16